

Answer ALL Questions

I-a) A sequential circuit has one J-K flip flop with output A and one D-flip flop with output B, one input Y, and one output Z. The flip flop input and output equations are as follows:

$$J_A = BY + \bar{B} \quad , \quad K_A = \bar{B}Y \quad , \quad D_B = \bar{A}Y \quad , \quad Z = AY + \bar{B}Y$$

i- Draw the logic diagram of the circuit, ii- Derive the state table, iii- Draw the state diagram.

b) With the aid of characteristic equations and truth tables, convert a D-type flip flop to (i) T-flip flop, (ii) JK flip flop.

II-a) Excess-3 code is generated by adding 3 to the BCD code. State a truth table showing the decimal digits 1, 2, 3, ..., 9, the corresponding BCD code, and the corresponding excess-3 code.

i- Design a combinational logic circuit that converts a 4-bit BCD input to its corresponding 4-bit excess-3 output. Implement your design using discrete AND, OR, XOR, and INVERTER gates.

ii- Implement the BCD-to-Excess-3 code converter in part (i) using programmable logic array (PLA) with 4-inputs and 4-outputs.

b) A BCD-to-Seven segment decoder is a combinational circuit that accepts a decimal digit in BCD and generates the appropriate outputs for selection of segments in a display indicator displaying the decimal digit. State a truth table for BCD-to-Seven segment decoder. Design and implement the corresponding combinational circuit using:

A programmable array logic (PAL) consisting of 4-inputs, 7-outputs, 7-sections each consisting of four-wide AND-OR array. One of the outputs is feed back to input.

III-a) Derive the synchronous input equations of a 4-bit synchronous binary counter based on D-type flip flops. Draw the corresponding counter circuit with the provision of Count Enable connection.

b) Design a combinational circuit that compares two 4-bit numbers A and B to check if they are equal. The circuit has one output Y so that Y=1 if A=B and Y=0 if A is not equal to B. Implement your design using discrete logic gates.

IV-a) Some microprocessors do not provide a separate address bus, instead they use the data bus for address transmission by multiplexing. With the aid of graphical illustration explain the multiplexed bus configuration system.

b) In a certain  $\mu P$ , the main program runs from address D110 to D193. Four nested subroutines have their start and end addresses as:

subroutine A  $\rightarrow$  A200 to A235

subroutine B  $\rightarrow$  A239 to A258

subroutine C  $\rightarrow$  C1A1 to C1A9

subroutine D  $\rightarrow$  C239 to C258

The BRANCH instructions are at the following addresses:

subroutine A  $\rightarrow$  D122

subroutine B  $\rightarrow$  A232

subroutine C  $\rightarrow$  A249

subroutine D  $\rightarrow$  C1A4

i- If the CPU internal stack registers are used, graphically show what the stack registers will contain after each push and pop operation.

ii- If a memory type stack whose addresses run from B138 to B13D (6-deep stack) is used. Graphically show the contents of the stack, the stack pointer, and program counter after all branches and returns for all four subroutines.

GOOD LUCK